### DATASHEET

#### 100 2500A PCI Express Protocol Analyzer - temp.pciea [not sav - D × File Configuration Capture Help Open 🕌 Save As 🛝 Capture 📰 Trigger 🕞 Start 📰 Stop 📝 Updates 😭 About Time Sequence # Requester ID / Tag Completer ID Address Item Data -327 0A00 (Bus:0A Dev:00 Fnc:0) / 00 Msg Transaction (Assert\_INTA) 137 0028 (Bus:00 Dev:05 Fnc:0) / 00 0A00 (Bus:0A Dev:00 Fnc:0) FBEFC044 4 bytes (76 00 00 00) MRd32 Transaction 518 518 0 DLLP (Ack) 518 62 0028 (Bus:00 Dev:05 Enc:0) / 00 0A00 (Bus:0A Dev:00 Enc:0) 4 bytes (76 00 00 00) TLP (CoID) 138 74 4<sup>11</sup> Msg Transaction (Deassert INTA) 139 0400 (Bus:04 Dev:00 Epc:0) / 00 99 EREECO44 4 hytes (EE EE EE EE) MRd32 Transaction 519 0028 (Bus:00 Dev:05 Enc:0) / 00 0A00 (Bus:0A Dev:00 Enc:0) 192 MsgD Transaction (Vendor\_Defined Type 1) 520 0000 (Bus:00 Dev:00 Enc:0) / 00 4 bytes (A4 00 00 00) 476 → MWr32 Transaction 521 0000 (Bus:00 Dev:00 Enc:0) / 0A EBEEC040 4 bytes (40.3C 21.00) 11 176 ⇒ MRd32 Transaction 141 0A00 (Bus:0A Dev:00 Fnc:0) / 00 0000 (Bus:00 Dev:00 Fnc:0) 00213C40 128 bytes (34 00 00 00 0A F. 11 376 DLLP (Ack) 141 11,452 → TLP (CpID) 522 0A00 (Bus:0A Dev:00 Fnc:0) / 00 0000 (Bus:00 Dev:00 Fnc:0) 64 bytes (34 00 00 00 0A F 11,478 → TLP (CpID) 523 0A00 (Bus:0A Dev:00 Fnc:0) / 00 0000 (Bus:00 Dev:00 Fnc:0) 64 bytes (00 20 00 14 00 D0. 11,500 + DLLP (Ack) 522 11,556 + DLLP (Ack) 11,578 523 ⇒ MRd32 Transaction 142 0A00 (Bus:0A Dev:00 Fnc:0) / 00 0000 (Bus:00 Dev:00 Fnc:0) 3C20B000 512 bytes (67 01 C7 5F 9B. 319,956 MRd32 Transaction 143 0A00 (Bus:0A Dev:00 Fnc:0) / 01 0000 (Bus:00 Dev:00 Fnc:0) 3C20B200 512 bytes (F2 09 46 E1 F9\_ 319,963 → MRd32 Transaction 144 0A00 (Bus:0A Dev:00 Fnc:0) / 00 0000 (Bus:00 Dev:00 Fnc:0) 3C20B400 512 bytes (EF 0A A6 8A AD... 320,482 MRd32 Transaction 145 0A00 (Bus:0A Dev:00 Fnc:0) / 01 0000 (Bus:00 Dev:00 Fnc:0) 3C20B600 512 bytes (C7 19 1B AA 7F... 320,489 MRd32 Transaction 146 0A00 (Bus:0A Dev:00 Fnc:0) / 00 0000 (Bus:00 Dev:00 Fnc:0) 3C20B800 512 bytes (97 FD B9 31 2C 321.008 MRd32 Transaction 147 0A00 (Bus:0A Dev:00 Fnc:0) / 01 0000 (Bus:00 Dev:00 Fnc:0) 3C20BA00 512 bytes (BC 60 AE 48 5C 321,015 HRd32 Transaction 148 0A00 (Bus:0A Dev:00 Enc:0) / 00 0000 (Bus:00 Dev:00 Enc:0) 3C20BC00 512 bytes (5D F7 6A EF 92 321.546 MRd32 Transaction 149 0A00 (Bus:0A Dev:00 Enc:0) / 01 0000 (Bus:00 Dev:00 Enc:0) 3C20BE00 512 bytes (EA C0 D2 9C 1A 321.553 → MRd32 Transaction 150 0A00 (Bus:0A Dev:00 Enc:0) / 00 0000 (Bus:00 Dev:00 Enc:0) 3C28C000 512 bytes (AD 29 74 D9 FD 322.084 ► MRd32 Transaction 151 0400 (Bus:04 Dev:00 Enc:0) / 01 0000 (Bus:00 Dev:00 Enc:0) 3C28C200 512 bytes (4C 46 B0 E0 E5 322 091 MRd32 Transaction 152 0400 (Bus:04 Dev:00 Enc:0) / 00 0000 (Bus:00 Dev:00 Enc:0) 3C28C400 512 bytes (4E ED EE 3B 5C 322 610 ⇒ MRd32 Transaction 153 0A00 (Bus:0A Dev:00 Enc:0) / 01 0000 (Bus:00 Dev:00 Enc:0) 3C28C600 512 bytes (AB 41 D3 60 18. 322,617 ⇒ MRd32 Transaction 154 0A00 (Bus:0A Dev:00 Fnc:0) / 00 0000 (Bus:00 Dev:00 Fnc:0) 3C28C800 512 bytes (4B 35 61 51 96... 323 316 0A00 (Bus:0A Dev:00 Fnc:0) / 01 0000 (Bus:00 Dev:00 Fnc:0) 3C28CA00 512 bytes (8E 65 39 3A B5 323.323 MRd32 Transaction 155 TLP (MRd32) Details Host to Device Link Direction Device to Host Link Direction Status Lane 0 Lane 1 Lane 2 Lane 3 Time Value Hep Status Lane 0 Lane 1 Lane 2 Lane 3 251 FB 3:3:3:3 00 00 00 3:3:3:3 00 00 raming STP 00 00 00 3:3:3:3 00 00 00 00 3:3:3:3 00 00 00 00 -10 518 0206 equence Numbe 518 3:3:3:3 00 00 00 00 3:3:3:3 00 00 00 00 -9 eader.Fmt 3 DW Header, No Data 0 0 3:3:3:3 00 00 00 00 3:3:3:3 00 00 00 00 -8 Header, Type MRd 0 00 3:3:3:3 00 00 00 00 3:3:3:3 00 00 00 00 Header.TC Traffic Class 0 0 0 3:3:3:3 00 00 00 00 3:3:3:3 00 00 00 00 -6 0 3:3:3:3 00 00 00 Header.TD TLP Digest/ECRC Not Present 0 00 00 3:3:3:3 00 00 00 -5 3:3:3:3 00 00 00 00 3-3-3-3 00 00 00 00 -4 Header FP TLP Not Poisoned 0 0 3333 00 00 00 00 00 3333 00 00 00 -3 Header.Attr Attributes: None 0 00 00 00 00 00 3:3:3:3 00 00 -2 Header.Length Transfer Size: 1 DWs 00 00 3-3-3-3 00 00 00 00 leader.1st DW BE 3:3:3:3 00 00 00 00 3:3:3:3 00 00 00 00 2.2.2 00 00 00 00 00 00 00 00 2500A PCI Express Protocol Analyzer 备 Protocol Ana (\*) International Test Instruments Corporation, California, USA Powe

### PCI EXPRESS 1.1 PROTOCOL ANALYZER 2500A

POCKET-SIZED PCI EXPRESS 1.1 PROTOCOL ANALYZER MODEL 2500A. SUPPORTS 2.5 GBPS WITH X1, X2 AND X4 LANE WIDTHS. FPGA-BASED, FULLY UPGRADEABLE DESIGN. REAL-TIME DATA CAPTURE AND DISPLAY. PC SOFTWARE INCLUDED. WORLD-WIDE SHIPPING.

> SUPPORTS ALL WINDOWS VERSIONS FROM XP TO 10 (32BIT/64BIT)

> > \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

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2500A PCI Express Protocol Analyzer - test.pciea

### DESCRIPTION

The 2500A PCI Express Protocol Analyzer supports the following features:

- ✓ PCI Express 1.1 (2.5 GBit/second) compliant
- ✓ User-selectable x4, x2 and x1 link width configurations.
- ✓ User-selectable 2 Gigabyte to 64 Kilobyte capture buffer. A selectable capture buffer size allows for smaller data files when saved to hard disk.
- A powerful 48 MHz Cypress FX2LP microprocessor implements on-demand upload of data via USB 2.0 after a completed capture. This allows you to immediately view data after the capture without having to wait for lengthy uploads of the full trace data.
- An Altera Arria II GX FPGA contains PCI Express x4 transceivers, a DDR2 Memory Controller and data upload interface to the micro-processor.
- Programmable Sequence Detectors allows the FPGA to detect the location of pre-defined as well as custom data sequences. This facilitates

Item		Sequence #	Requester ID .	/Tag		Completer ID	Address	Data		Status	Time	
🗉 🕂 Msg Transaction (Assert_INTA)		871	0A00 (Bus:0A Dev:00	Fnc:0) / 00							0.000 ns	
TLP (Msg: Assert_INTA)		871	0A00 (Bus:0A Dev:00	) Fnc:0) / 00							0.000 ns	
DLLP (Ack)		871	100 C			-		-			324.000 ns	
🗲 MRd32 Transaction		469	0028 (Bus:00 Dev:05	Fnc:0) / 00	04 🏹	Hide Protocol Iterr	is of This Type	00 00 00)			1.348 us	
→ TLP (MRd32)		469	0028 (Bus:00 Dev:0	5 Fnc:0) / 00	10	Show All Protocol	ltems	uested			1.348 us	
🗲 DLLP (Ack)		469				Copy to Clipboard	Ctrl+C				1.596 us	
← TLP (CpID)		872	0028 (Bus:00 Dev:05	Fnc:0) / 00	04 49			00 00 00)			1.644 us	
		873	0400 (Bus:04 Dev:00			Select All	Ctrl+A				1.744 us	
🖃 🗲 MRd32 Transaction		470	0028 (Bus:00 Dev:05	Fnc:0) / 00	۵۵ 🖵	Add Marker		F FF FF)			2.220 us	
→ TLP (MRd32)		470	0028 (Bus:00 Dev:05	Fnc:0) / 00	_	Edit Marker		ested			2.220 us	
		470			×					2.468 us		
		874	0028 (Bus:00 Dev:05	Fnc:0) / 00	04 📉	Delete Marker	F FF FF)			2.516 us		
		874			×	Delete All Markers					2.836 us	
		471	471 0000 (Bus:00 Dev:00		- #3	Search Payload Da	6	0 00 00)			3.404 us	
	DLLP (Ack) Deta	ails						Cur	rent	Previous	Next	
Name		Value	Dec Hex	🖃 🔶 H2D F	Proti 🍓	Print Protocol Viev	/ Items	07	1	Go to Previous	Go to Next	
aming	SDP		92 5C	🕀 🕂 H		Export Protocol Vie	w Items to XML	73	1	Go to Previous	Go to Next	
DLLP Type Ack			0 00	🗉 📑 H	2D	•		86	1	Go to Previous	Go to Next	
••	871		871 367	. ⊞ 1111 H		Set Time Reference	2	48	1	Go to Previous	Go to Next	
kNak_Seq_Num				🖃 🔶 D2H F	Prote 🔭	Clear Time Referer	ice	16	1	Go to Previous	Go to Next	
c	OK		5,084 13DC	🗄 🕂 D				01	1	Go to Previous	Go to Next	
aming	END		253 FD	🗉 🔂 D	2Н 🔟	Absolute Time		93	1	Go to Previous	Go to Next	
				🗉 🖽 🗹	2H	Relative Time		22	1	Go to Previous	Go to Next	
						Show Time in Tick						
						Show Time In thek	,					

hardware-acceleration of PCI Express Protocol Item detection after capture. This, in turn, enables the software to display the data very quickly after a completed capture without a need for the software to locate the PCI Express Packets and Ordered Sets captured.

- An 8-level trigger with up to 2048 byte deep data detection per trigger level allows triggering on very long data sequences. In total, data sequences up to 16 Kbytes in length can be triggered upon.
- ✓ A TTL-compatible Trigger in / out port allows synchronization with external test instruments.
- ✓ A x4 slot probe with a 1 m (3.3ft) cable is included. 3<sup>rd</sup> party, custom probes can also be designed and connected to the 2500A unit.
- Microprocessor firmware and FPGA configuration are automatically updated with the PC application software. No separate and complex hardware re-programming is needed.
- Overall, the 2500A hardware and software has been designed for maximum efficiency and simplicity of use. The hardware is small enough to fit in your pocket, the software is very easy to use but yet the complete package is very flexible and powerful.

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### UNIQUE ADVANCED FEATURES

- The Hierarchical Protocol Tree View organizes the captured PCI Express protocol data into a format that exactly reflects the nesting of the actual protocol items on the bus. This greatly eases understanding of the PCI Express protocol. Other PCI Express Protocol Analyzers use a primitive block-type display which makes it very hard to see the overall hierarchy of the complex data being communicated.
- FPGA hardware acceleration (indexing) of protocol items allows instantaneous Protocol View display after custom filtering, even for a full 2 gigabyte capture. Other Protocol Analyzers use the computer's CPU to parse the captured data which is orders of magnitude slower.
- Idle Data Hardware Filtering allows capture of minutes worth of link data, allowing tens of millions of protocol items to be captured. This will allow you to capture rare or unknown events that are otherwise impossible to set up trigger conditions for.
- Dynamic on-demand data upload from the hardware allows effortless access to and

Item		Sequence #	Requester ID / Tag			Completer ID			Add	ress	Data		Status		Time		_
🛯 🚭 Msg Transaction (Asser	LINTA)	871	0A00 (Bus:0A De	v:00 Fnd	= ::0) / 00											-337	
↓ <sup>11</sup> TLP (Msg: Assert_I	NTA)	871	0400 (Bus:04 De	ev:00 Fnd	:0) / 00											-337	
<ul> <li>DLLP (Ack)</li> </ul>		871														-256	
🛛 🗲 MRd32 Transaction		469	0028 (Bus:00 De	v:05 Fnc	:0) / 00	0A00 (Bus:	0A Dev:0	0 Fnc:0)	FBEF	044	4 bytes (D4 00 00 00)					0	
→ TLP (MRd32)		469	0028 (Bus:00 De	ev:05 Fr	nc:0) / 00				FBEF	-0 <b>0</b>	4 bytes requested					0	
🔶 DLLP (Ack)		469														62	
← TLP (CpID)		872	0028 (Bus:00 Dev:05 Fnc:0) / 00			0A00 (Bus:0A Dev:00 Fnc:0)				4 bytes (D4 00 00 00)						74	
🗄 🕂 Msg Transaction (Deassert_INTA)		873	0A00 (Bus:0A Dev:00 Fnc:0) / 00													99	
🖃 🗲 MRd32 Transaction		470	0028 (Bus:00 Dev:05 Fnc:0) / 00			0A00 (Bus:0A Dev:00 Fnc:0)			FBEF	FBEFC044 4 bytes (FF FF FF FF)					218		
<ul> <li>TLP (MRd32)</li> </ul>		470	0028 (Bus:00 De	v:05 Fnc	:0) / 00				FBEF	C044	4 bytes requested					218	
🔶 DLLP (Ack)		470														280	
← TLP (CpID)		874	0028 (Bus:00 De	v:05 Fnc	:0) / 00	0A00 (Bus:	0A Dev:0	0 Fnc:0)			4 bytes (FF FF FF FF)					292	
Item Marker Text			Time V		Host to Device Link [			Direction	n	C	Host Link	ist Link Direction					
Msg Transaction (Assert_I	NT M1		-337			Status	Lane O	Lane 1	Lane 2	Lane	3 Status	Lane O	Lane 1	Lane 2	Lane 3	Time	,
TLP (MRd32)	Trigger		0	_		3333	00	00	00	00	3:3:3:3	00	00	00	00		
MWr32 Transaction	P1		1,541,462	Е	Edit Ma	irker		00	00	00	3:3:3:3	00	00	00	00		
MWr32 Transaction	P2		1,542,457		Delete	Marker		00	00	00	3:3:3:3	00	00	00	00		
MRd32 Transaction	M2		23,916,328	×	Delete A	All Markers		00	00 00	00	3:3:3:3	00	00	00	00		-2
MRd32 Transaction M3			181,115,825					00	00	00	3:3:3:3	00	00	00	00		
				T <sub>o</sub>		ie Reference	20	01	D5	00	3:3:3:3	00	00	00	00		
				76	Clear T	ime Referen	ce	00	01	00	3:3:3:3	00	00	00	00		
				~	Ahsolu	te Time		00	OF	FB	3:3:3:3	00	00	00	00		
								C0	44	51	3:3:3:3	00	00	00	00		
					Relativ	: iime		90	D8	END	3:3:3:3	00	00	00	00		

browsing of gigabyte sized trace data without a need to first upload the complete data to the PC. Only the part of the Protocol View that is actually visible will result in data fragments being uploaded from the 2500A unit.

- Extremely deep Trigger Sequence Detectors allow detection of eight trigger levels of up to 2,048 bytes per level or in total 16 kilobytes. Other Protocol Analyzers normally only allow you to trigger on a few DWords of packet payload data.
- Multiple time-correlated views of the data are simultaneously available, allowing you to easily see transaction, packet and lane details from the highest to lowest abstraction levels at a glance. Some other PCI Express Protocol Analyzers require you to change the protocol view to view the data at a different abstraction level, resulting in lengthy reparsing of the data as well as loss of situational awareness of your location within the overall trace.
- Hardware acceleration of Protocol Item detection allows immediate display of the number of each type of protocol item in the trace as well as immediate jump to or filtering of any protocol item type.
- The 2500A unit is significantly smaller than competing PCI Express Protocol Analyzers, allowing it to be easily transported in your pocket or laptop bag (dimensions/ weight is only 4.90" x 4.10" x 1.4" / 16oz or 125 x 105 x 35 mm / 450g).

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### SOFTWARE OVERVIEW

The 2500A software supports the following features:

- ✓ The trigger position can be adjusted within the capture buffer (i.e. pre or post trigger).
- ✓ Lane Polarity, Lane Mapping and Descrambling can be adjusted / disabled as needed.
- The software dynamically acquires the data required to display the visible part of the trace as the data is browsed. This results in very quick and effortless browsing of the captured data regardless of the capture buffer size used.
- Multiple Views of the data are time-correlated; the Protocol View displays a hierarchical view of all Transactions as well as the Packets included within the transactions; the Lane View displays the raw data and control characters as they were received on the link under test; finally, the Detail View decodes details of the packet selected in the Protocol View. Together, these views give you a quick and easy way to browse the captured data from the highest to lowest information level.

III 2500A PCI Express P	rotocol Analyzer - test.pcie	ea [not saved]												
File Configuration	Capture Help													
늘 Open 🕌 Save A	s 🔹 Capture 📒 Trig	gger 🛛 💽 Sta	art 🔳 Stop 🛛 🛃	Updates 🕤 Ab	out									
	Item	Sequence #	Requester II		Complet	er ID	Address		Data		S	atus	Time	*
😑 🕂 Msg Transaction (A		871	0A00 (Bus:0A Dev:	00 Fnc:0) / 00				~						337
← <sup>M</sup> TLP (Msg: Ass	ert_INTA)	871	Sapture Configu	uration			×							337
→ DLLP (Ack)		871	<ul> <li>Trigger Position with</li> </ul>	hin Capture Buffer									-1	256
MRd32 Transaction		469	riggor contorrina	in oup and band			OK	tes (D4 00 00 00)				0		
→ TLP (MRd32		469					Cancel	tesre	quested					
DLLP (Ack)		469 872	Beginning		End		Cancer		4 00 00 00	a				62 74
← TLP (CpID)	Desseet INTA)	873						tes (D4	+ 00 00 00	J				99
Msg Hansaction (E)		470	Capture Buffer Size	Link Width				tes (FF	FF FF FF	1				218
→ TLP (MRd32)		470	2 Gigabyte     ▼     Disable Descrambling     tes requested										218	
DLLP (Ack)		470	2 digabyte	*	•	Uisabie	e Descramping							280
← TLP (CpID)		874	Invert Polarity on TI	hese Lanes				tes (FF	FF FF FF	1				292 👻
TLP (MRd32) Details		H2D Lane 0 H2D Lane 1 H2D Lane 2 H2D Lane 3 Device to Host Link Direction												
Name	Value	Dec	D2H Lane 0	D2H Lane	1 🔲 D2H	ane 2	D2H Lane 3		Status	Lane 0	Lane 1	Lane 2	Lane 3	Time
Framing	STP								3:3:3:3	00	00	00	00	-5
Sequence Number	469		Lane Mapping						3:3:3:3	00	00	00	00	-4
Header. Fmt	3 DW Header, No Data		Standard	Reversed	🔘 Custo	m (drag-and-	drop below)		3:3:3:3	00	00	00	00	-3
Header. Type	MRd							-	3:3:3:3	00	00	00	00	-2
			H2D Lane Order:	0123	D2H Lan	e Order: 🛛 🕕	123		3:3:3:3 3:3:3:3	00	00	00	00	-1
Header.TC	Traffic Class 0								3:3:3:3	00	00	00	00	1
Header.TD	TLP Digest/ECRC Not								3:3:3:3	00	00	00	00	2
Header.EP	TLP Not Poisoned		0	0	3:3:3:3 EF	CO	44 51		3:3:3:3	00	00	00	00	3
Header.Attr	Attributes: None		0	0	3:3:3:3 99	90	D8 END		3:3:3:3	00	00	00	00	4
Header.Length	Transfer Size: 1 DWs		1	1 -	•	1			1					•
🔎 Details View 🏦 S	iearch View 📃 Markers Vi	ew			👔 Node Fin	der 010 Pa	yload View 🏨 L	ane Viev	v					
Protocol Analyzer Disc	onnected													

- All Protocol Items in the trace are displayed in the 'Node Finder' View. This view allows direct jump to any protocol item in the trace. The Node Finder can also be used to hide / show packets of a particular type.
- The 'Search View' allows you to search for binary or string data in packet payload. Multiple searches can be started and run in the background as you continue working with the software. The Search View allows direct jumps to the search result locations.
- The 'Markers View' displays the trigger position as well as any markers you have added to the capture. Markers are saved with the project and allow you to quickly locate interesting areas in the trace at a later time.
- Protocol Item Filtering allows you to instantly hide any given Protocol Item Type from the Protocol View. Due to the dynamic data access of the Protocol View, filtering is very quick, even for a full 2 Giga-byte capture.
- The Protocol View and Lane View data can be exported to file in XML format and to the clipboard in CSV format. This allows easy post-processing of the captured data via your own or 3<sup>rd</sup> party software.
- Time can be shown in absolute (measured from capture start) or relative (measured from prior protocol item) mode.

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